What is claimed is:

1. A frame number detecting device, comprising:

frame number detecting means receiving an input signal comprising a sector containing data of a plurality of frames, each said frame comprising frame number information recorded as a sync signal used to specify the number of said frame in said sector, said frame number detecting means detecting said numbers of said frames by using said sync signal of said input signal;

first and second counters which increment their count numbers in accordance with input of said sync signal, wherein when said count numbers have reached a given value, said first and second counters return said count numbers to zero and then increment said count numbers again in accordance with the input of said sync signal;

comparing means for comparing the value of said number of said frame read by said frame number detecting means and the value of said count number of said first counter to see whether the values agree with each other; and

state detecting means which causes a state variable to vary on the basis of the result of comparison made by said comparing means, wherein when said state variable satisfies a given condition, said state detecting means causes said first counter to change the value of said count number to the value of said number of said frame read by said frame number detecting means without incrementing said count number, and when said state variable satisfies another given condition, said state detecting means causes said second counter to change the value of said count number to the value of said count number of said first counter without incrementing said count number,

and wherein said frame number detecting device outputs the value of said count number of said second counter as said number of said frame.

2. The frame number detecting device according to claim 1,

wherein said sync signal comprises a plurality of types, and

said frame number detecting means detects said numbers of said frames by using part of combinations of said types of said sync signal in successive two or more of said frames.

3. The frame number detecting device according to claim 2,

wherein said frame number detecting means comprises,

sync signal type detecting/encoding means for specifying said type of said sync signal and outputting said type in an encoded form,

a latch circuit for latching an output from said sync signal type detecting/encoding means, and

sync number encoding means for detecting a combination of variation of said types of said sync signal of successive two or more of said frames by using an output from said sync signal type detecting/encoding means or/and an output from said latch circuit, specifying said number of said frame by using said part of said combinations, and encoding said number of said frame.

4. The frame number detecting device according to claim 3, wherein

said frame number detecting means further comprises converting means for converting said input signal into a plurality of pieces of parallel data having the same contents, and

said sync signal type detecting/encoding means comprises,

sync signal type detecting means comprising a plurality of detectors, said

plurality of detectors respectively receiving said pieces of said parallel data and specifying said type of said sync signal in said parallel data, and

sync signal type encoding means for encoding an output from said sync signal type detecting means and outputting the encoded type.

5. The frame number detecting device according to claim 3, wherein said frame number detecting means comprises a plurality of said latch circuits.

6. The frame number detecting device according to claim 1, wherein said state detecting means comprises,

an up/down counter receiving said result of comparison made by said comparing means, said up/down counter increasing/decreasing its count number in accordance with said result of comparison and outputting said count number as said state variable,

a first gate circuit composed of a combination of a plurality of gate circuits, said first gate circuit causing its output signal to go active when said state variable has reached a given value,

a second gate circuit composed of a combination of a plurality of gate circuits, wherein when said state variable has reached another given value, said second gate circuit causes its output signal to go active and outputs said output signal to said second counter, thereby causing said second counter to change the value of said count number to the value of said count number of said first counter without incrementing said count number, and

a third gate circuit, wherein when said frame number detecting means has detected said number of said frame and the output signal of said first gate circuit has become active, said third gate circuit causes its output signal to go active and outputs said

output signal to said first counter, thereby causing said first counter to change the value of said count number to the value of said number of said frame read by said frame number detecting means without incrementing said count number.

7. The frame number detecting device according to claim 1,

wherein said state variable can take at least three values, and

when said result of comparison made by said comparing means indicates a mismatch, said state detecting means causes the value of said state variable to vary in an increasing or decreasing direction, and when said result of comparison made by said comparing means indicates a match, said state detecting means causes the value of said state variable to vary in a direction opposite to the direction adopted in the case of said mismatch,

and wherein said given condition is a condition in which said frame number detecting means was able to detect said number of said frame and said state variable has reached a given value, and

said another given condition is a condition in which said state variable has reached another given value.

8. The frame number detecting device according to claim 1, further comprising timing adjusting means for adjusting timing of operations of said frame number detecting means, said first and second counters and said state detecting means by using said sync signal.

9. The frame number detecting device according to claim 8, further comprising,

sync signal detecting/securing means for detecting said sync signal and outputting a pulse corresponding to said sync signal, wherein when said sync signal is lacking, said sync signal detecting/securing means inserts an interpolating sync signal pulse, and

masking means for blocking the output of said pulse for a given period after said sync signal detecting/securing means has outputted one pulse.

10. The frame number detecting device according to claim 9, wherein said masking means comprises,

edge detecting means receiving said pulse outputted from said sync signal detecting/securing means, for detecting an edge of said pulse,

a counter which, when receiving an output of said edge detecting means, outputs another pulse having a larger pulse width than said pulse and then ceases outputting said another pulse until certain times of clock have been inputted even if supplied with said output of said edge detecting means, and

an AND gate receiving said pulse and said another pulse as its inputs.